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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,633	12/29/2000	Michael C. Panis	1473-US	9260

7590 03/11/2005

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,633	PANIS ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3 May and 24 Sept. 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicants' amendments of 3 May and 24 Sept. 2004.

1.1 **Claims 1, 2, 4, 8, 12** and **20** are amended, **Claims 10-11** are cancelled. **Claims 1-9** and **12-20** remain pending.

1.2 The objections of record are withdrawn in response to Applicants' amendment.

1.3 The art rejections of record are maintained in response to Applicants' amendment.

Response to Arguments

2. Applicants' arguments have been fully considered but they are not persuasive.

REMARKS

2.1 In response to **Claims 1-9** and **12-20**, Applicants allege, on page 3 para. 2 et seq.: remarks' section of the amendment of 3 May 2004, that the prior art of record does not teach: transmission line characteristic evaluation or jitter pattern insertion because the prior art of record only relates to self-testing.

Examiner disagrees and notes that the prior art of record does not restrict test implementation exclusively to a self-testing structure with specific stimulus application types.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.1 **Claims 1-9, 12-20** are rejected under 35 U.S.C. 102(b) as being anticipated by **Ramamurthy et al.** (US Patent No. 5,790,563) and **Bell et al.** (US Patent No. 5,875,293).

a. **As per Claims 1-9, 12-20, Ramamurthy et al.** discloses equivalent means for testing serial ports e.g., in Fig. 1, comprising receiver and transmitter configured to effect parametric/functional testing in Fig. 2:block 50, with means to selectively apply direct input or output of said receiver in e.g., Abstract and col. 2 line 29, col. 4 line 35 et seq., lines 50-55; with programmable threshold means in e.g., Fig.1: Block 24, Fig. 2:Block 50, or col. 2 line 20 et seq., loop back means in Fig. 1 numerals 34-34a and col. 4 line 1 et seq.; comparison means to decide error-free condition in col. 5 line 2 et seq.

Ramamurthy et al. discloses that other user defined tests in e.g., col. 2 line 30, well known in the art can be performed, such as timing characteristics diagnosis as admitted by applicant as prior art in page 5 line 19 and Fig. 1.

b. **As per Claims 1-9, 12-20, Bell et al.** discloses equivalent means for testing serial ports e.g., in Figs. 1-6, comprising receiver and transmitter configured to effect parametric/functional testing with means to selectively apply direct input or output of said receiver in e.g., Abstract and with programmable threshold means, loop back means; comparison means to decide error-free condition, e.g., '*The dual serial port device 244 is then tested to verify functionality. This is a closed loop test where the host computer 104 is involved. In general, both of the COM1 and COM2 serial ports 244a, 244b will be used where one is being tested while the other is used as a synchronization port. The synchronization port is preferably set with the same baud rate, data bits and stop bits as is used during the driver and host communication in the test loop. It is noted that since the COM1 serial port 244a has already been used for communications with the host computer 104, it has already been tested with certain limited functionality of the CTS/RTS and SIN/SOUT signals. Therefore, the COM2 serial port 244b is the initial port tested while the COM1 serial port 244a serves as the synchronization port... The first test performed for serial communications is an internal loop back test, which is used to verify the internal operation of a universal asynchronous receiver transmitter (UART) including register data lines and internal signal routing. Then a control input lines test is used to verify that the input lines to the test UART are operational. In this test, the host computer 104 toggles the input*

control lines of the UUT 100 in a predetermined order. The test begins with the UUT 100 sending a control input lines test message to the host computer 104 via the synchronization port. The host computer 104 then sets a first bit pattern onto the serial port being tested and responds with an OK message on the synchronization port. The UUT 100 verifies the settings and responds by sending an OK message to the host computer 104. If an error is found, the UUT 100 sends a TEST COMPLETED message to complete the particular test routine. For the control input lines test, DCD, RI, DSR, and CTS signals are tested. Then, the control output lines test is performed in a similar manner, where the UUT 100 toggles the output control lines of the UART under test in a particular order, which is verified by the host computer 104. If an error is found, the host computer 104 sends a TEST COMPLETED message to the UUT 100 and the test routine is terminated. For this test, the RTS and DTR signals are tested. Data transmission and receive tests are then performed to verify the transmission and receive capability of the UARTS at various baud rates. Preferably, the UUT 100 configures the serial port being tested for several baud rates, including baud rates of 300, 2400, 9600 and 19200 bits per second (bps). For the transmission tests, the UUT 100 sends data bytes 0-FFh as quickly as the port is able to handle and then waits for the host computer 104 to respond. Similarly, during the receive test the host computer 104 sends data bytes as quickly as the port under test can accept them and then sends an OK message to the UUT 100, where the UUT 100 then responds with a test result.'

Bell et al. discloses that other user defined tests in e.g., col. 18 line 28 et seq., well known in the art can be performed, such as timing characteristics diagnosis as admitted by applicant as prior art in page 5 line 19 and Fig. 1.

Conclusion

4. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
3/7/05